UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/915,707	07/25/2001	Amit Dhir	X-880 US	9378

24309 7590 02/14/2005

XILINX, INC
ATTN: LEGAL DEPARTMENT
2100 LOGIC DR
SAN JOSE, CA 95124

EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 02/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/915,707	DHIR ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-13* is/are rejected.

7)☒ Claim(s) *5* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/25/2001*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 6-8, 12 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Pat. No. 6,080,203 to Njinda et al. (hereafter Njinda).

3. As per claim 1, Njinda discloses a programmable logic integrated circuit (Fig. 1, Column 5, lines 12-18), and used in a communication system (network communication system), comprising: at least a first and a second physical layer module (Fig. 1, elements 26) each can interact with a physical medium under a predetermined specification (Ethernet type connections follow particular specifications, e.g., 100BaseT, etc., Column 4, 40-50); a media independent interface that can receive a first set of data from either one of the first and the second physical layer modules (Fig. 1, element 28) and generate a second set of data (second set of data is the data that goes from element 28 to element 62 in Fig. 2A); and a media access control module (Fig. 2A, element 62) that processes the second set of data.

4. As per claim 8, Njinda discloses a programmable logic integrated circuit (Fig. 1, Column 5, lines 12-18) used in a communication system (compute network communication system), comprising: a physical layer module (Fig. 1, elements 26) that can interact with a physical medium under a predetermined specification (100BaseT, Ethernet specification); and at least a first and a second media access control module (Fig. 2, specifically Fig. 2A, element 62 and Fig.

2B, element 62) that can receive and process data from the physical layer module (data from the PHY module received through MII modules, element 28).

5. As per claims 6,7 and 12,13, Njinda discloses claims 1 and 8, wherein the MII and MAC are home phone line networking specification or the Ethernet specification (Column 4, lines 40-50, home phones can use Voice over IP, working over internet connections using Ethernet, see attached reference by How Networks Work, pg 69). Furthermore, it is inherent various other communication specifications one wishes to use dependent upon the application can be used. Computer networks are formed using various disparate communication specifications including wireless specifications (see attached reference by How Networks Work, pgs 114-115).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2-4 and 9-11 are rejected under 35 USC 103(a) as being unpatentable over US Pat. No. 6,080,203 to Njinda et al. (hereafter Njinda) in view of US Pat. No. Re. 34,363 to Freeman.

8. As per claims 2-4 and 9-11, Njinda discloses claims 1 and 8, respectively.

Njinda does not disclose expressly the MAC module and the first and second physical modules being embedded in the programmable logic fabric or interconnect logic layer separating the fixed logic component from the programmable logic fabric, or the interconnect logic layer

comprises interconnecting tiles, although Njinda infers a programmable logic fabric it in the RTL code shown in Columns 13-32.

Freeman discloses a FPGA where the realization of the programmable code Njinda discloses is implemented via electronic design automation techniques so that the code is realized as hardware on the FPGA, e.g., on the programmable hardware logic fabric (Fig. 4A). As shown in Fig. 4A, there is a programmable logic fabric in which fixed logic components (elements 40-1 thru 40-9) are separate from the interconnecting mesh (construed as the tiles) that connect the fixed logic components.

Njinda and Freeman are analogous art because they are from the same field of endeavor in implementing logic on a single chip in order to be incorporated into an overall system.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to implement logic onto the programmable logic fabric of an integrated circuit such as an FPGA.

The suggestion/motivation for doing so would have been the RTL code that Njinda shows which can be downloaded, converted, place and routed onto the hardware logic of an FPGA via electronic design automation techniques which are well known in the art.

Therefore, it would have been obvious to combine Njinda with Freeman for the benefit of transferring hardware logic implemented via software language such as Verilog into hardware realization on a chip.

Allowable Subject Matter

9. Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, an integrated circuit as claimed in claim 2, wherein the MAC module comprises a first portion and a second portion, wherein the first portion remains unchanged after configuration and the second portion is partial reconfigurable based on the selection of the first or second physical layer module.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following patents are cited to further show the state of the art with respect to programmable logic circuits used in a network environment:

U.S. Pat. No. US 20020078249A1 to Lu et al.

U.S. Pat. No. US006167403A to Whitmire et al.

U.S. Pat. No. US006067585A to Hoang

U.S. Pat. No. US006243756B1 to Whitemire et al.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 571-272-4143. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on (571) 272-4146. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
2/10/2005

JEFFREY GAFFIN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100